Figure 1

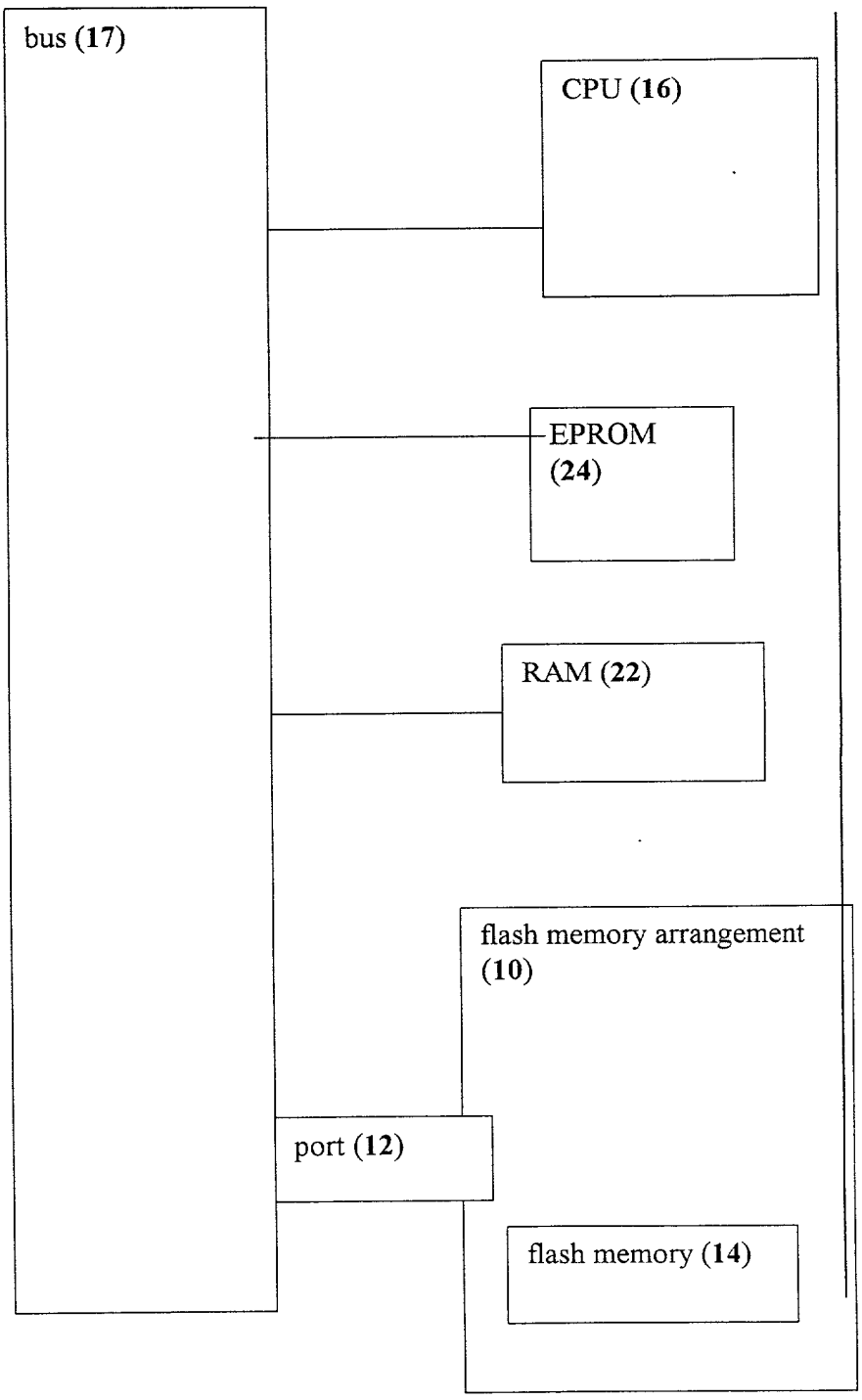

bus (17)
CPU (16)
EPROM (24)
RAM (22)
flash memory arrangement (10)
port (12)
flash memory (14)

Figure 2

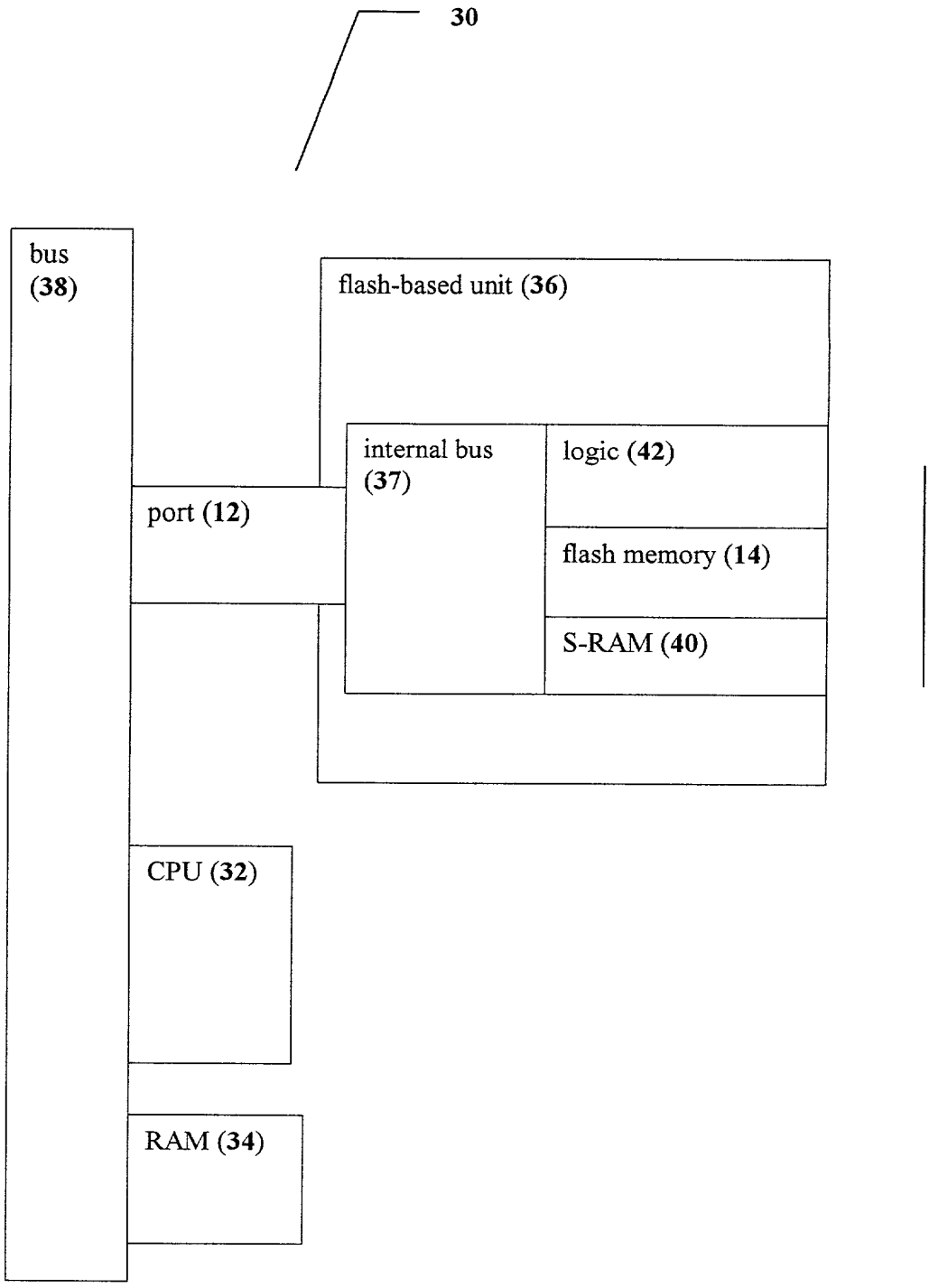

30
bus
(38)
flash-based unit (36)
internal bus
(37)
logic (42)
port (12)
flash memory (14)
S-RAM (40)
CPU (32)
RAM (34)

Figure 3

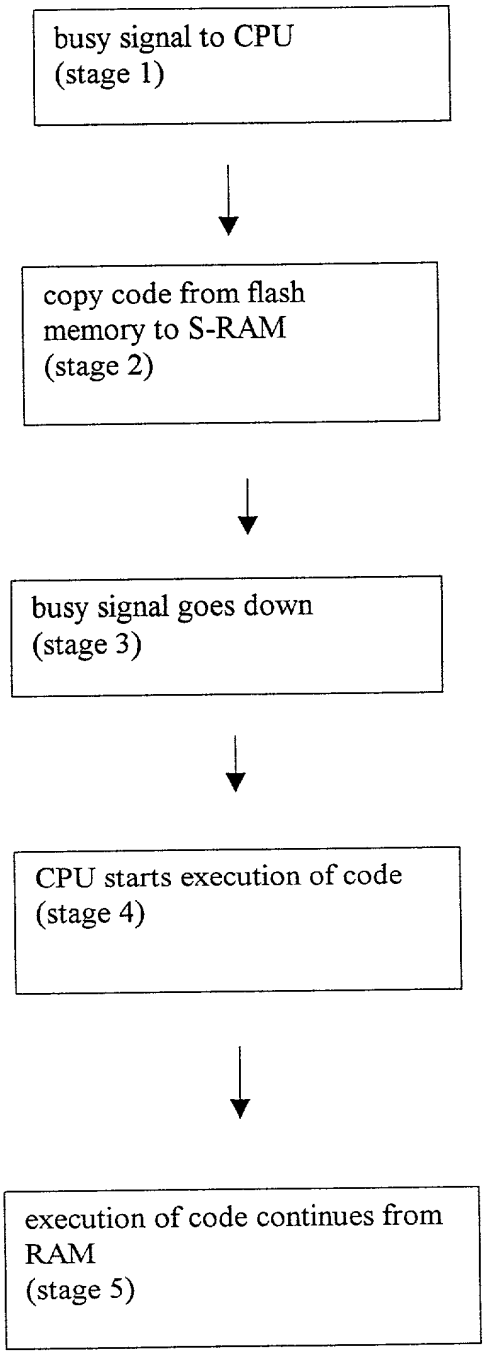
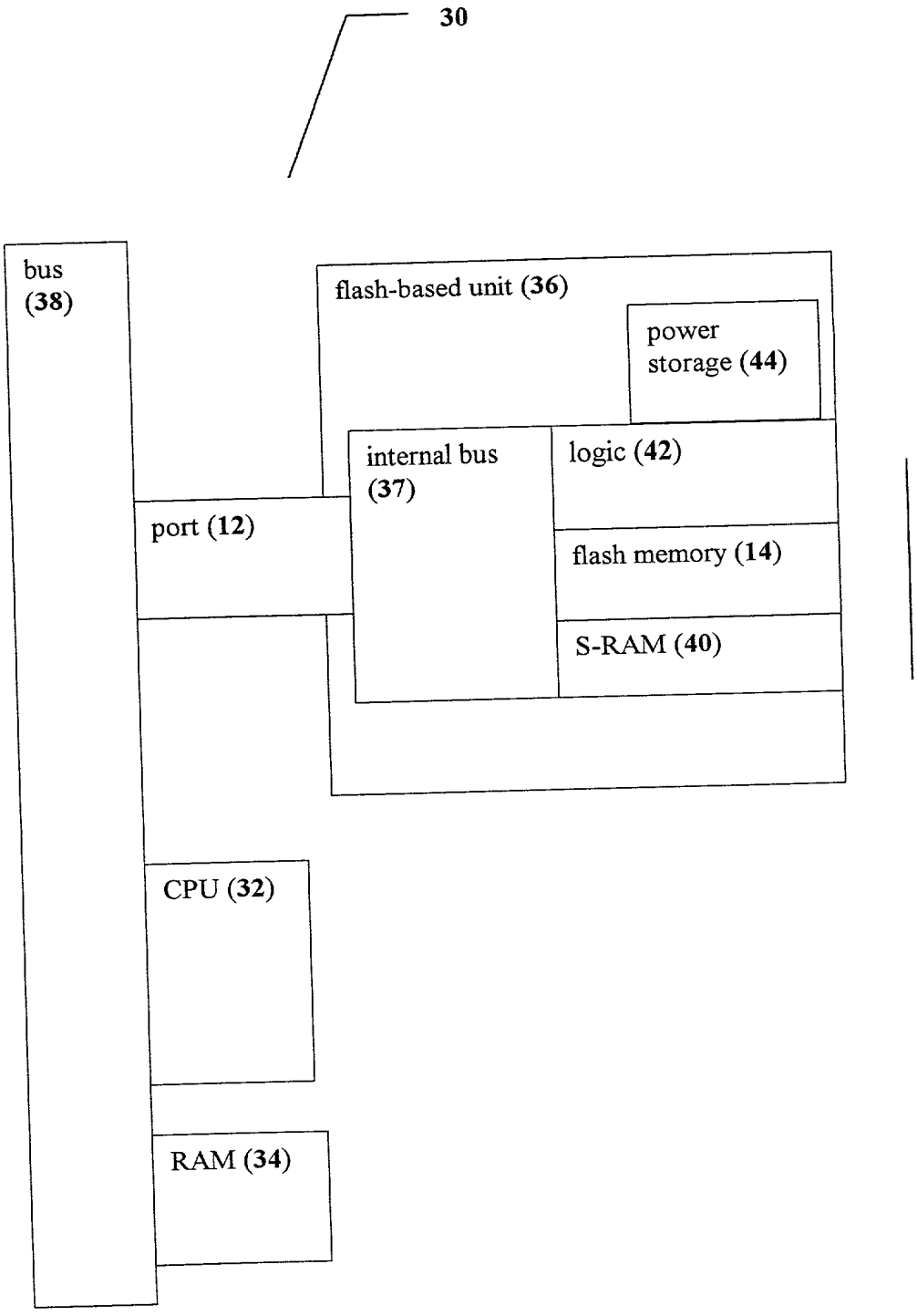

busy signal to CPU
(stage 1)
copy code from flash
memory to S-RAM
(stage 2)
busy signal goes down
(stage 3)
CPU starts execution of code
(stage 4)
execution of code continues from
RAM
(stage 5)

Figure 4


30
bus
(38)
flash-based unit (36)
power
storage (44)
internal bus
(37)
logic (42)
port (12)
flash memory (14)
S-RAM (40)
CPU (32)
RAM (34)